REMARKS

Applicants thank the Examiner for acknowledging receipt of Applicants' foreign priority documents that have been submitted pursuant to 35 U.S.C. §§119 and 120.

Applicants respectfully request reconsideration of the prior art rejection set forth by the Examiner under 35 USC §§102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone or in combination, fail to either teach or suggest Applicants' presently claimed invention. Applicants' claimed invention is directed to an improved solid state image sensor device and method of driving a solid state image sensor device which is capable of operating in both an interlaced mode and a progressive mode wherein all of the signal charges are read out from the imaging device independently without being combined.

As described in the specification, in the progressive mode, reading out of image signals is performed such that all picture element signals are independently output without being mixed. In contrast, in the interlaced scanning mode, 525 scanning lines are scanned alternately such that a first field and a second field are obtained by respective scannings and the respective fields are superimposed in order to obtain a frame of an image.

One of the deficiencies of the conventional driving techniques for solid state imaging devices is that in the progressive mode, one signal for each picture element is output so that the saturation signal quantity becomes half of that compared with the interlaced mode of operation. The saturation signal quantity is the maximum signal quantity that may be achieved when the solid state image sensor device outputs the correct signal. In the conventional mode of operation, during progressive output, there is a decrease in the

saturation signal quantity which results in the degradation of the dynamic range for the device.

Applicants have overcome the shortcomings of the prior art by providing image scanning techniques which rely upon the application of voltage to the substrate such that during the progressive mode of operation, the substrate voltage is smaller than the bias voltage applied during the interlaced mode of operation. See, for example, each of the independent claims and the summary of the invention. Applicants have demonstrated that the improve dynamic range results in a much more capable device that provides high quality image output regardless of the mode of operation.

Applicants submit that the prior art references of record fail to provide any teaching or suggestion whatsoever regarding Applicants' advance in the art. More specifically, Applicants note that the Fukuba United States Patent No. 5,523,787 is merely directed to a solid state imaging device comprising a full frame transfer vertical shift register wherein signal charges are stored in two sections. Two vertically adjacent pixels are consecutively transferred to a horizontal shift register while the horizontal shift register is not operated in order to mix the signal charges together. See, for example, the abstract of the disclosure in the Fukuba reference.

There is no teaching or suggestion whatsoever in Fukuba regarding the application of a substrate voltage. In recognition of this deficiency, the Examiner relies on the teachings of the Suzuki reference, United States Patent No. 5,828,407. However, this reference is directed to the operation of an imaging device in a field mode and a frame mode wherein during operation in the frame mode, a potential of the substrate of the image sensing device and an intermediate voltage of pulses that are applied to the vertical transfer unit are set to potentials that are lower than those in the field mode of operation.

Moreover, Suzuki merely teaches that by changing the substrate potential, it is possible to drain away undesired charge into the silicon substrate which is much different from the present invention wherein the substrate bias voltage is applied during the progressive mode of operation such that a potential difference is generated between a doped region and a well of the photodiode which is greater than during interlaced operation. Applicants have added new claims that underscore these distinctions. The specific details concerning this aspect of the Applicants innovation are found in the specification on page 11 beginning in the second full paragraph and carrying over to page 12. It is this particular potential difference that enables the improved operational characteristics of the claimed photodiode structures. Suzuki fails to provide any teaching or suggestion whatsoever regarding this advance in the art.

More specifically, at best, Suzuki merely teaches that adjustment of a potential wall can be used to selectively drain away undesired charge. See col. 3 lines 20-40. In contrast, Applicants have discovered that in using a photodiode structure, a variation in the potential difference between a doped region and a well of the photodiode can be used to alter the ability to accumulate signal charge and the dynamic range of the device during different types of operation. No portion of Suzuki or any other reference of record teaches this significant improvement for imaging devices employing photodiode structures.

Accordingly, in light of the foregoing, Applicants respectfully submit that the references of record fail to provide the requisite teaching or suggestion to support the rejection of the claims as set forth by the Examiner. Applicants respectfully request that the Examiner now withdraw these rejections and allow all claims in the application.

Respectfully submitted,

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CERTIFICATE OF MAILING

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